Claim 1(amended). A MOS transistor in a single-transistor memory cell, comprising:

a semiconductor substrate having a substrate surface, a first conductive region and a second conductive region;

a gate oxide disposed on said substrate surface;

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having at least one side wall adjacent at least one of said conductive regions; and

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an insulating silicon nitride spacer disposed on said side wall of said gate, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate.

Claim 3(amended). The MOS transistor according to claim 1,

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wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

Claim 4(amended). The MOS transistor according to claim 1, wherein said gate includes a tungsten silicide layer and a polysilicon layer.